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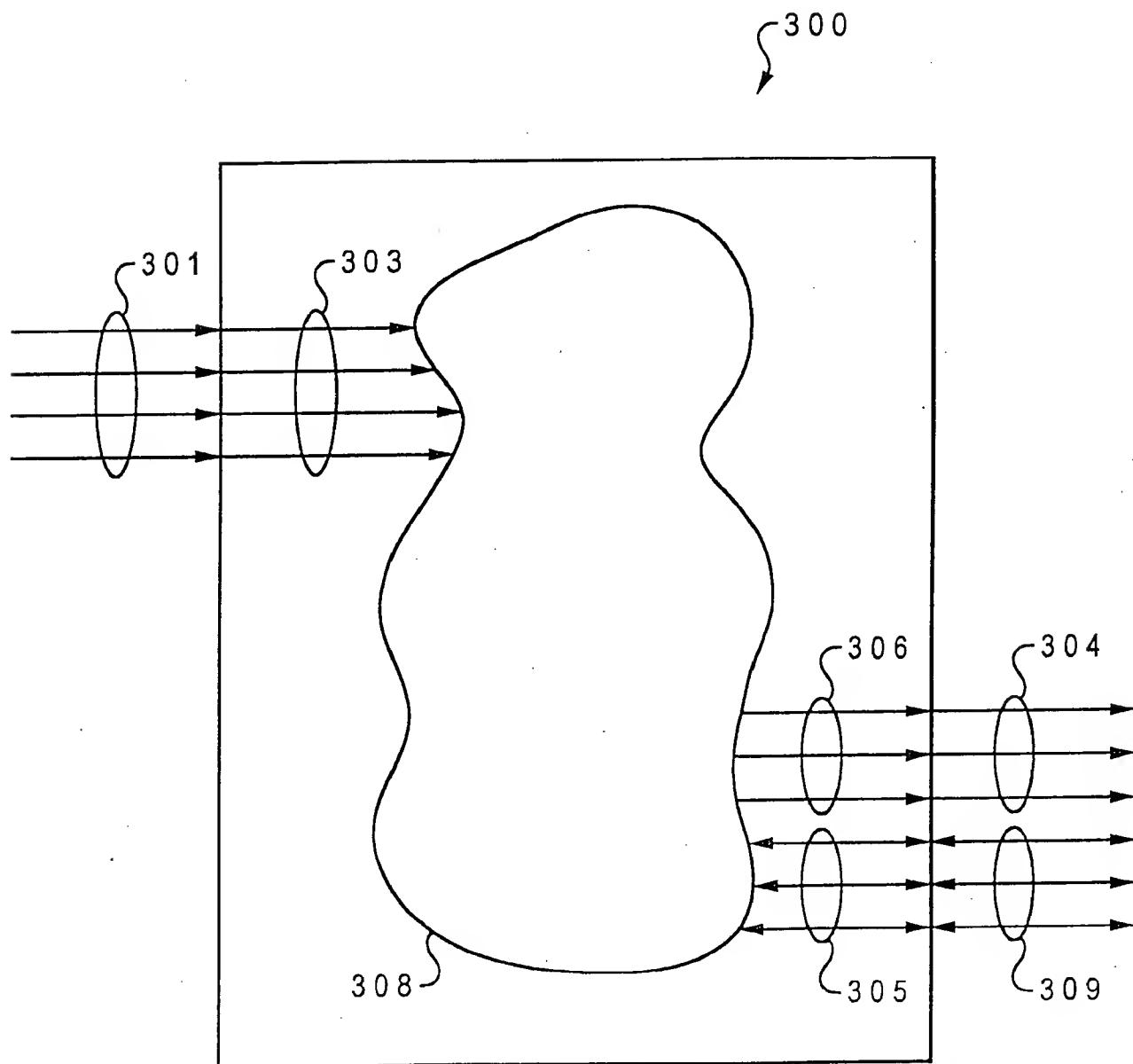


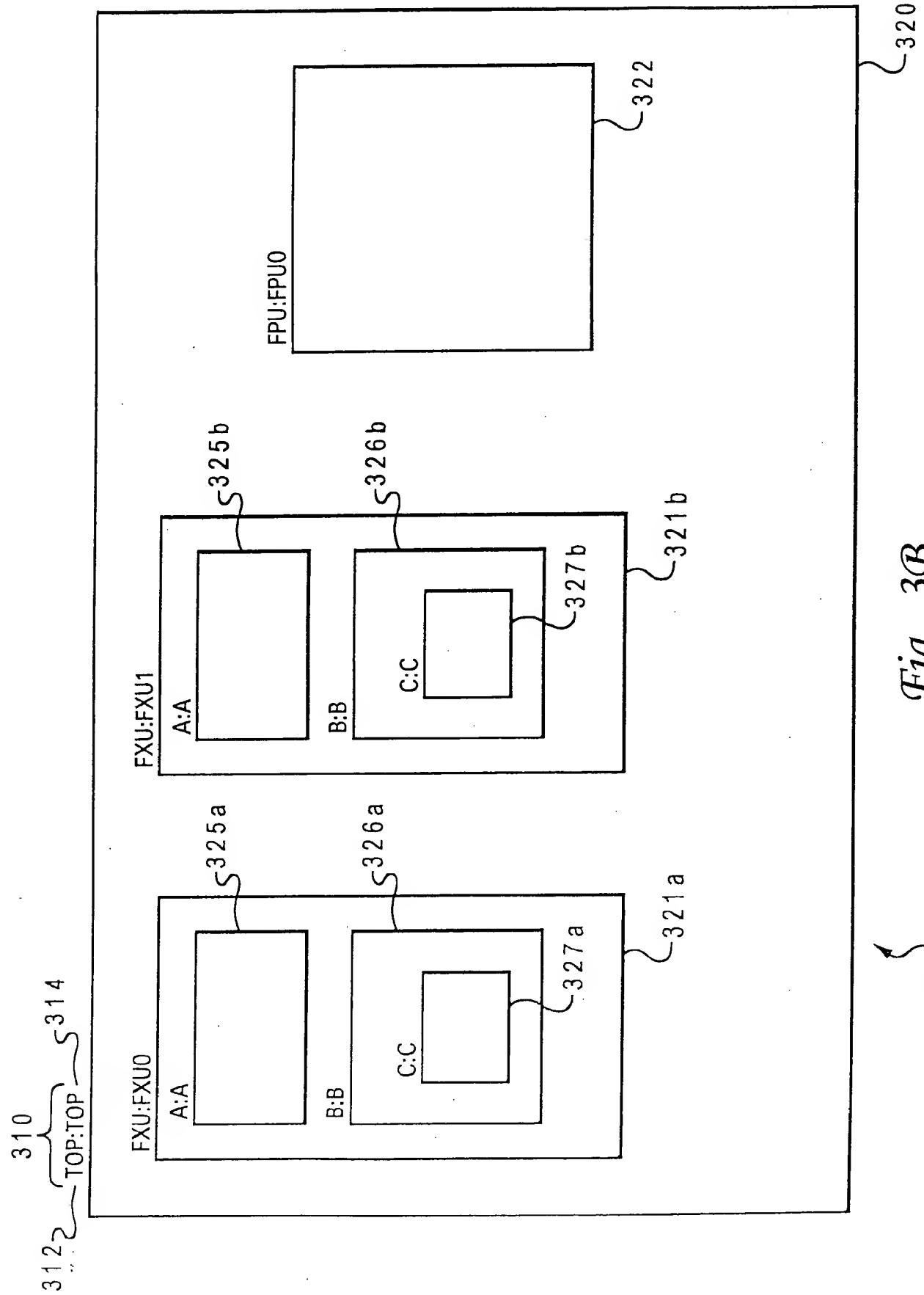
Fig. 3A
Prior Art

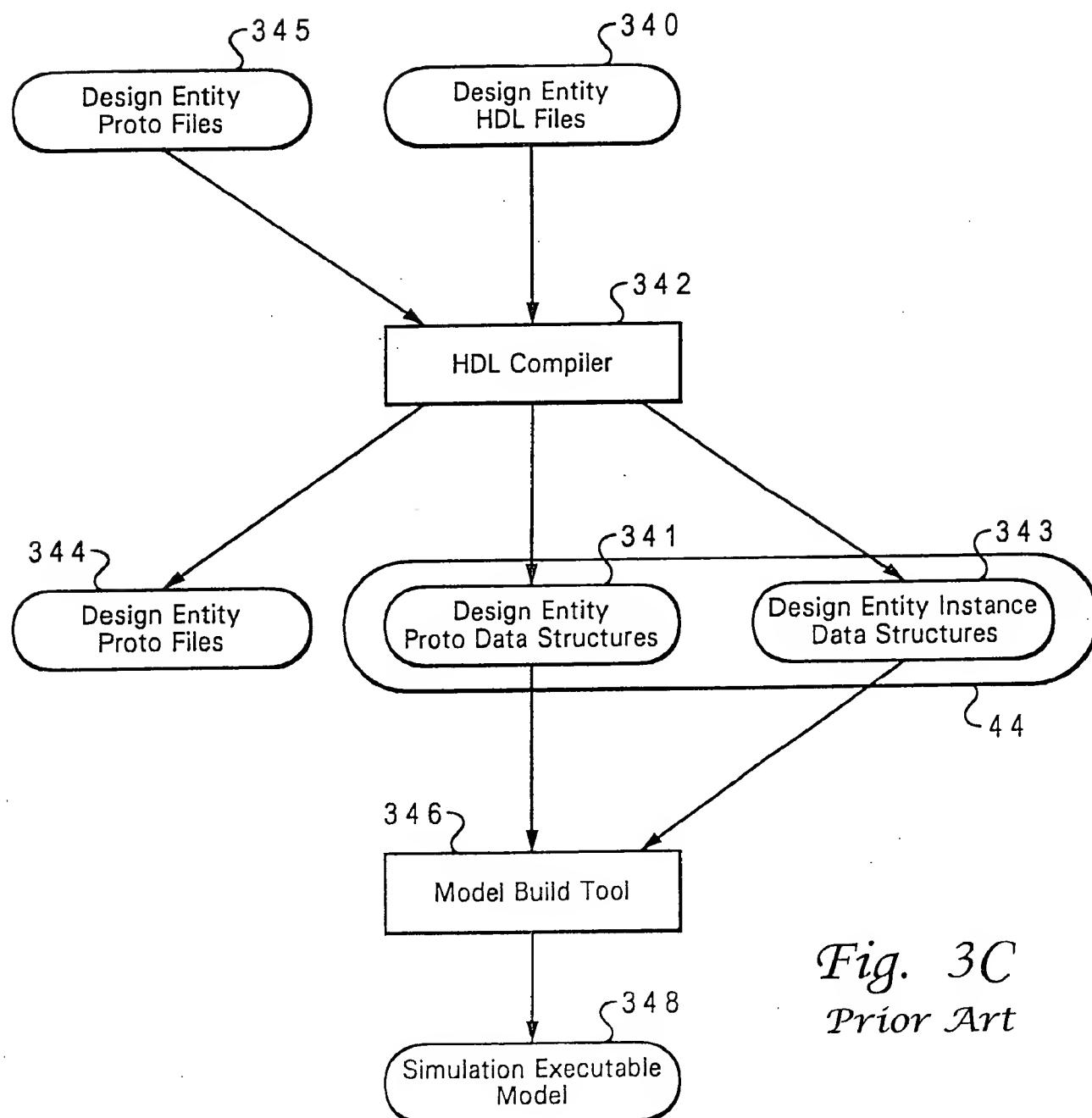
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Fig. 3B
Prior Art



*Fig. 3C
Prior Art*

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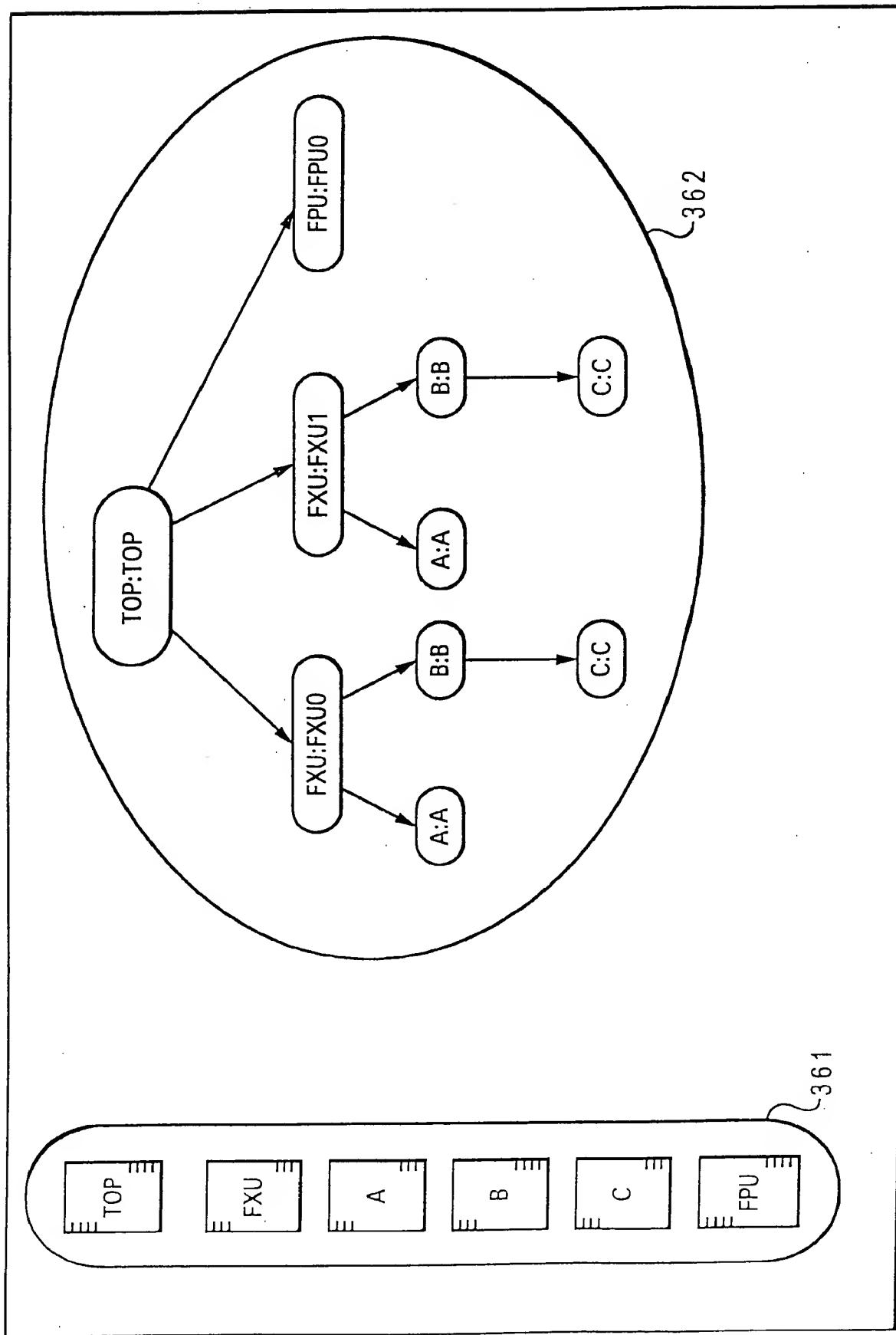


Fig. 3D
Prior Art

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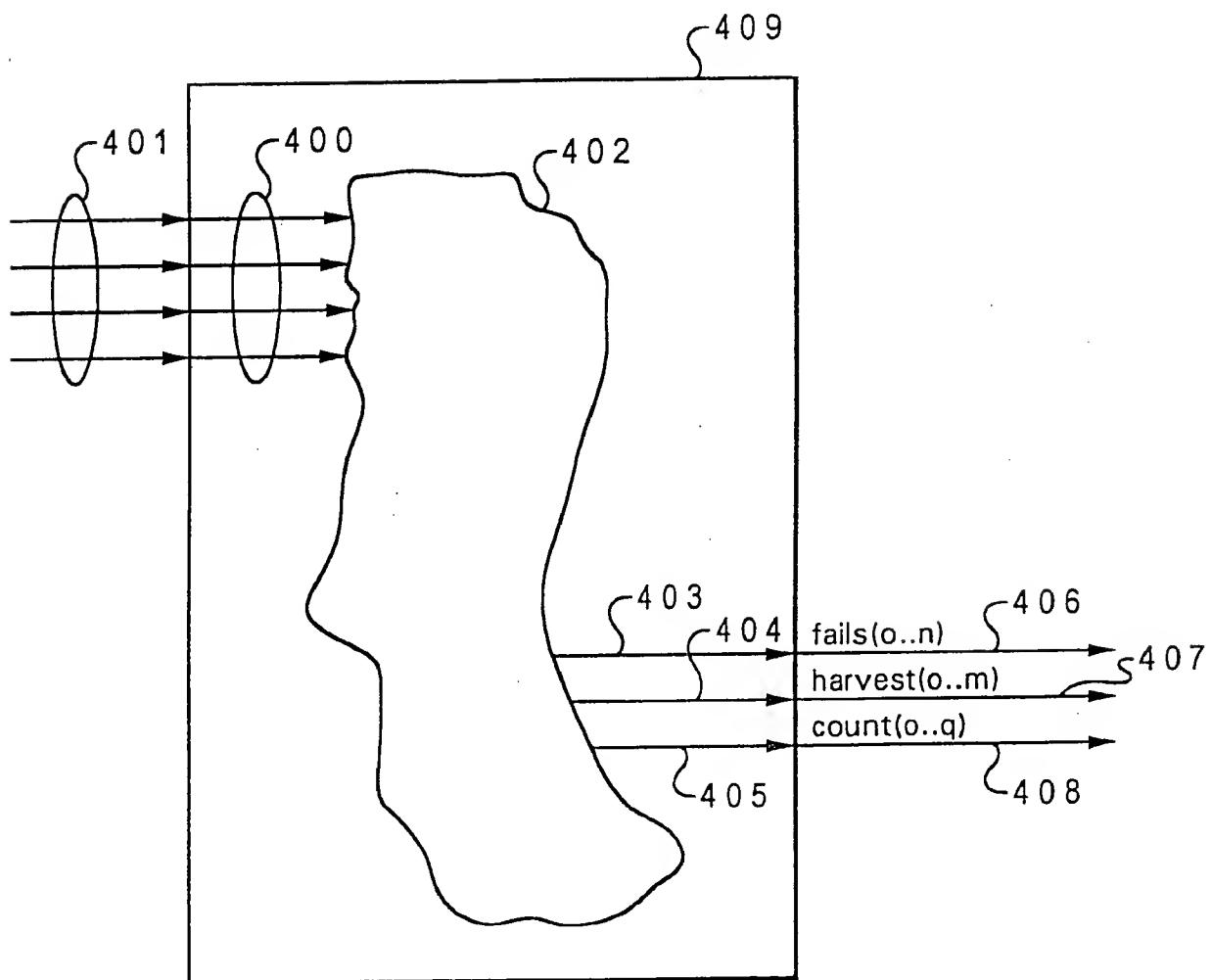


Fig. 4A
Prior Art

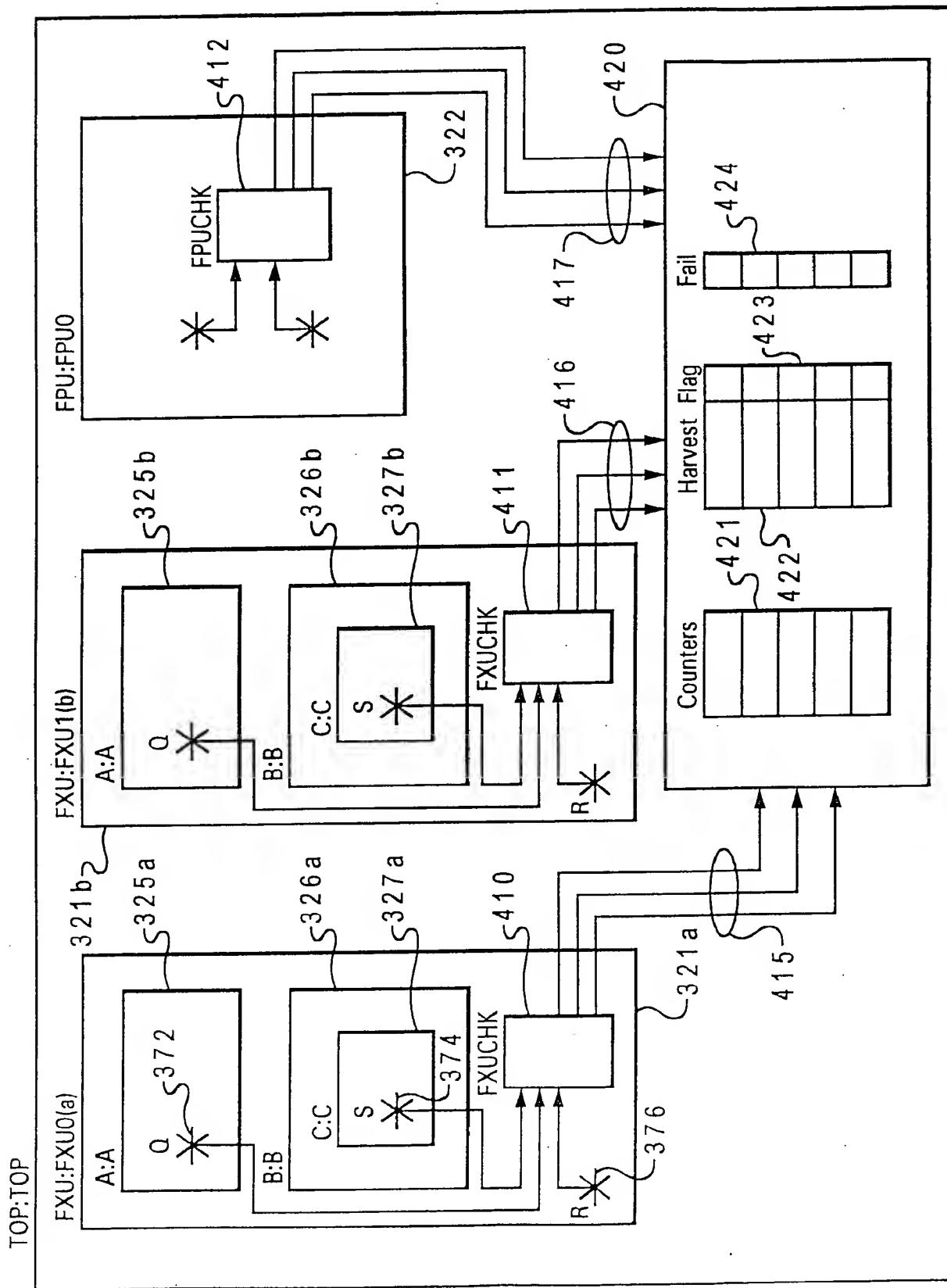


Fig. 4B
Prior Art

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ENTITY FXUCHK IS

```

  PORT( S_IN      : IN std_ulogic;
         Q_IN      : IN std_ulogic;
         R_IN      : IN std_ulogic;
         clock     : IN std_ulogic;
         fails     : OUT std_ulogic_vector(0 to 1);
         counts    : OUT std_ulogic_vector(0 to 2);
         harvests  : OUT std_ulogic_vector(0 to 1);
);
  
```

450 } 450

452 { --!! BEGIN
 --!! Design Entity: FXU;

453 { --!! Inputs
 --!! S_IN => B.C.S;
 --!! Q_IN => A.Q;
 --!! R_IN => R;
 --!! CLOCK => clock;
 --!! End Inputs

454 { --!! Fail Outputs;
 --!! 0 : "Fail message for failure event 0";
 --!! 1 : "Fail message for failure event 1";
 --!! End Fail Outputs;

455 { --!! Count Outputs;
 --!! 0 : <event0> clock;
 --!! 1 : <event1> clock;
 --!! 2 : <event2> clock;
 --!! End Count Outputs;

456 { --!! Harvest Outputs;
 --!! 0 : "Message for harvest event 0";
 --!! 1 : "Message for harvest event 1";
 --!! End Harvest Outputs;

457 { --!! End;

440 } 451

458 } 458

ARCHITECTURE example of FXUCHK IS

```

BEGIN
  ...
  ... HDL code for entity body section ...
END;
  
```

Fig. 4C
Prior Art

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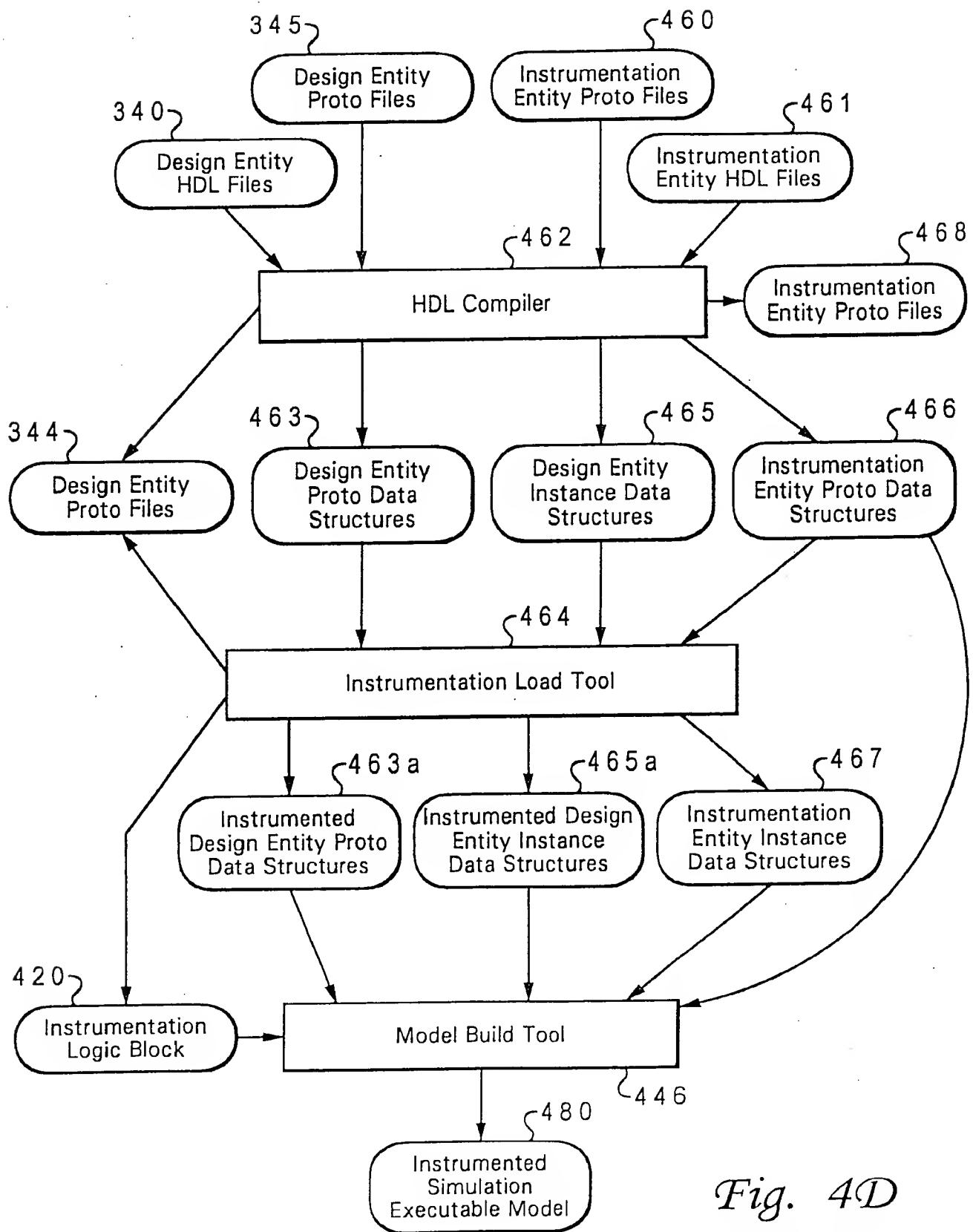


Fig. 4D
 Prior Art

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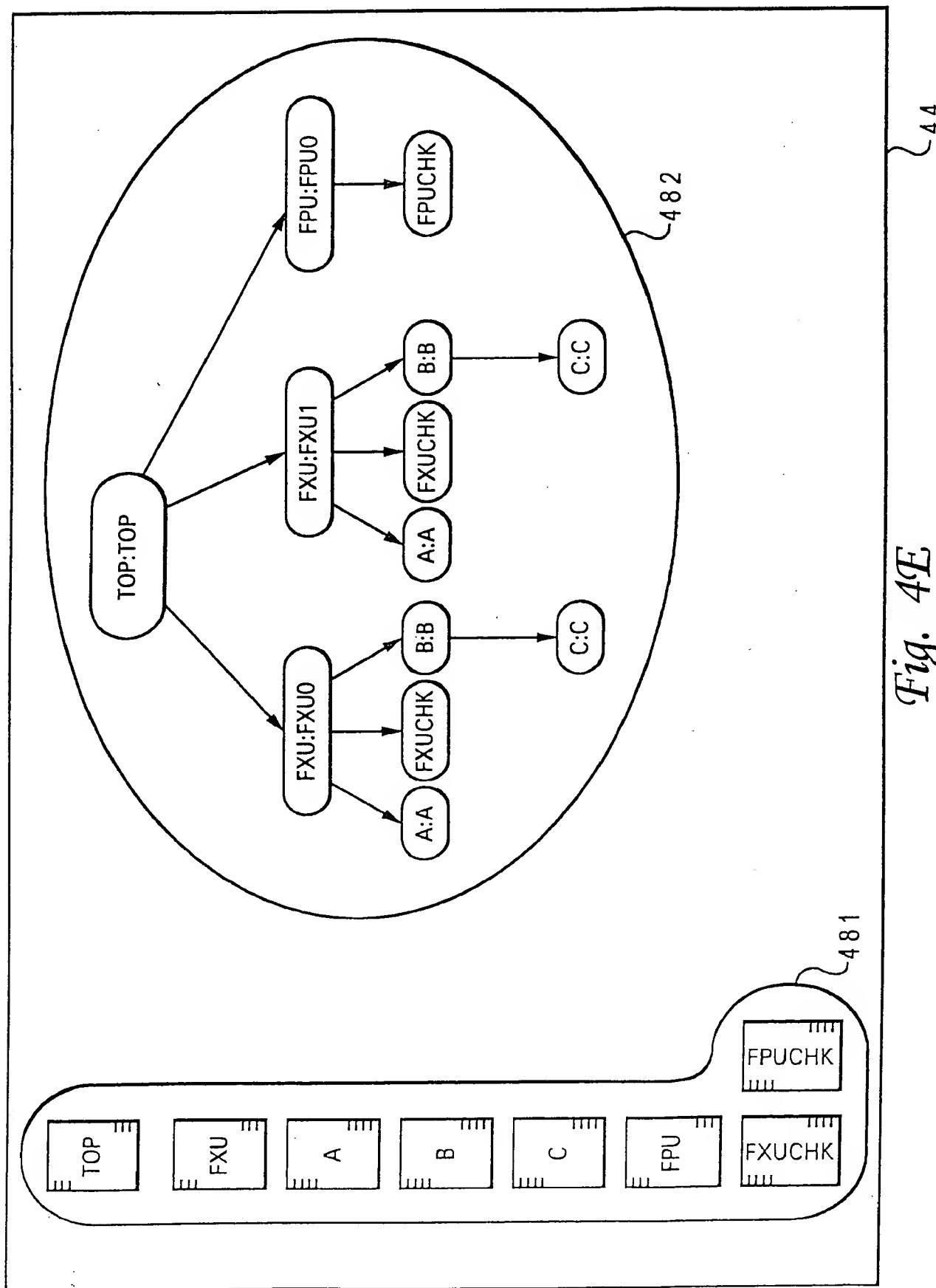


Fig. 4E
Prior Art

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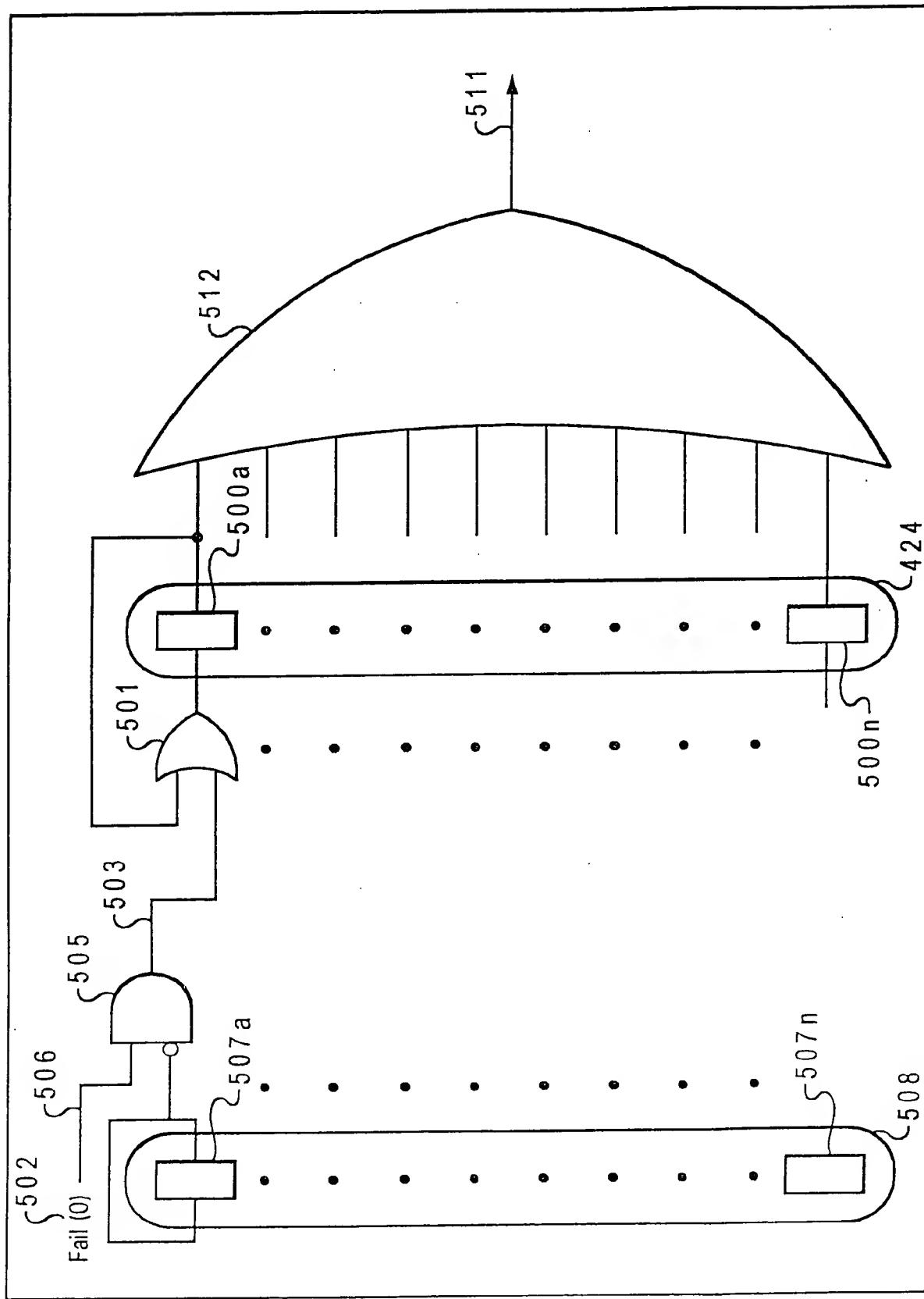


Fig. 5A
Prior Art

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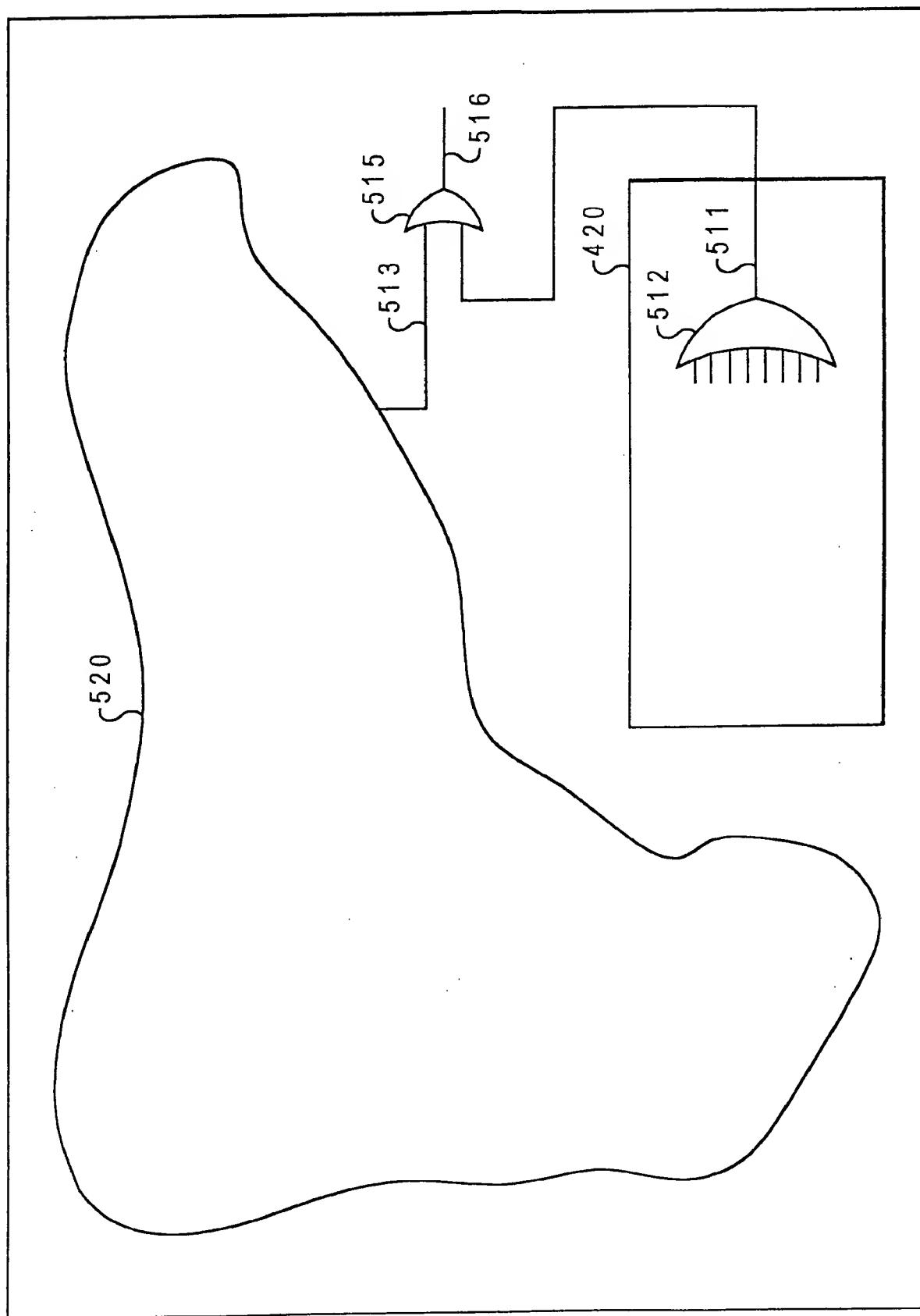
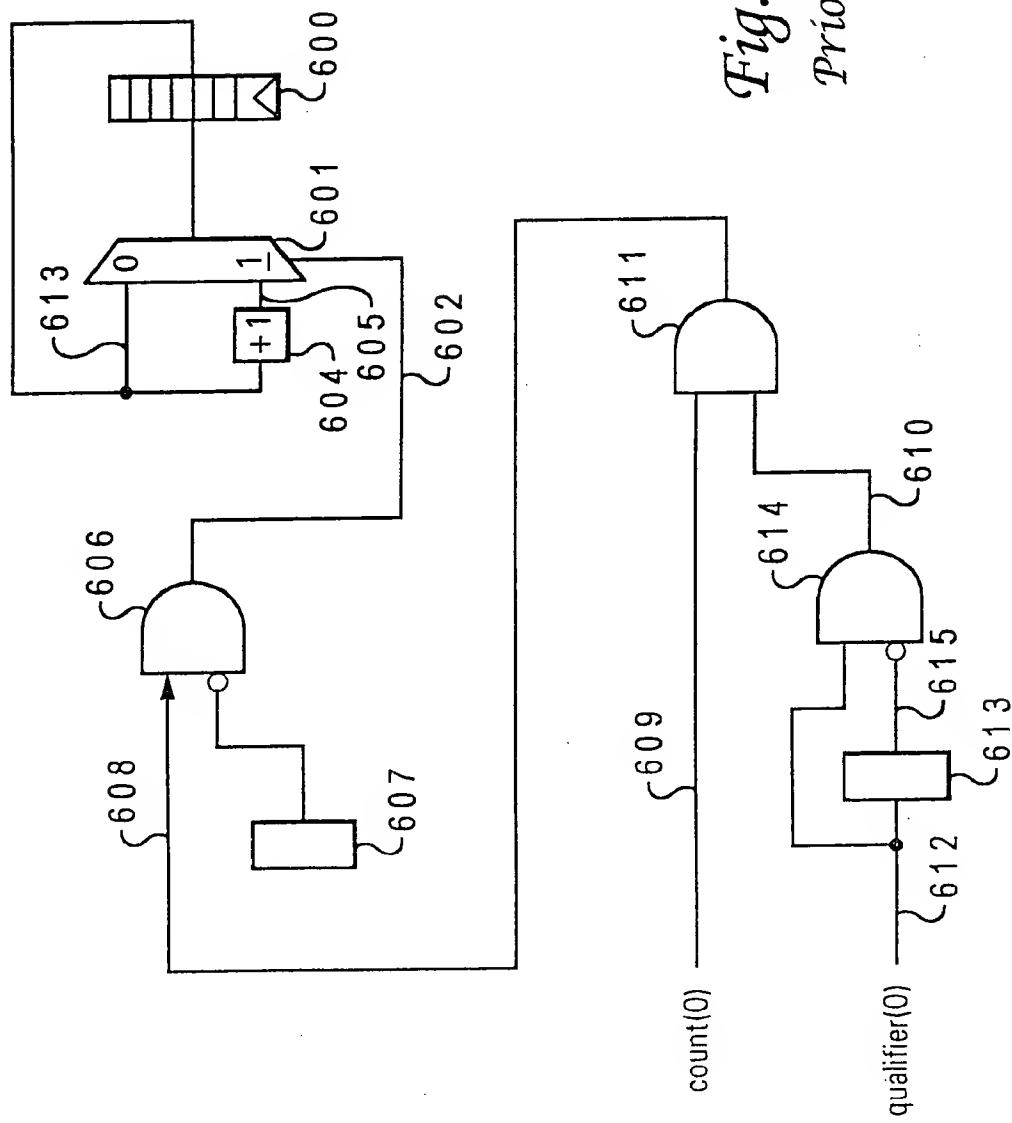


Fig. 5B
Prior Art

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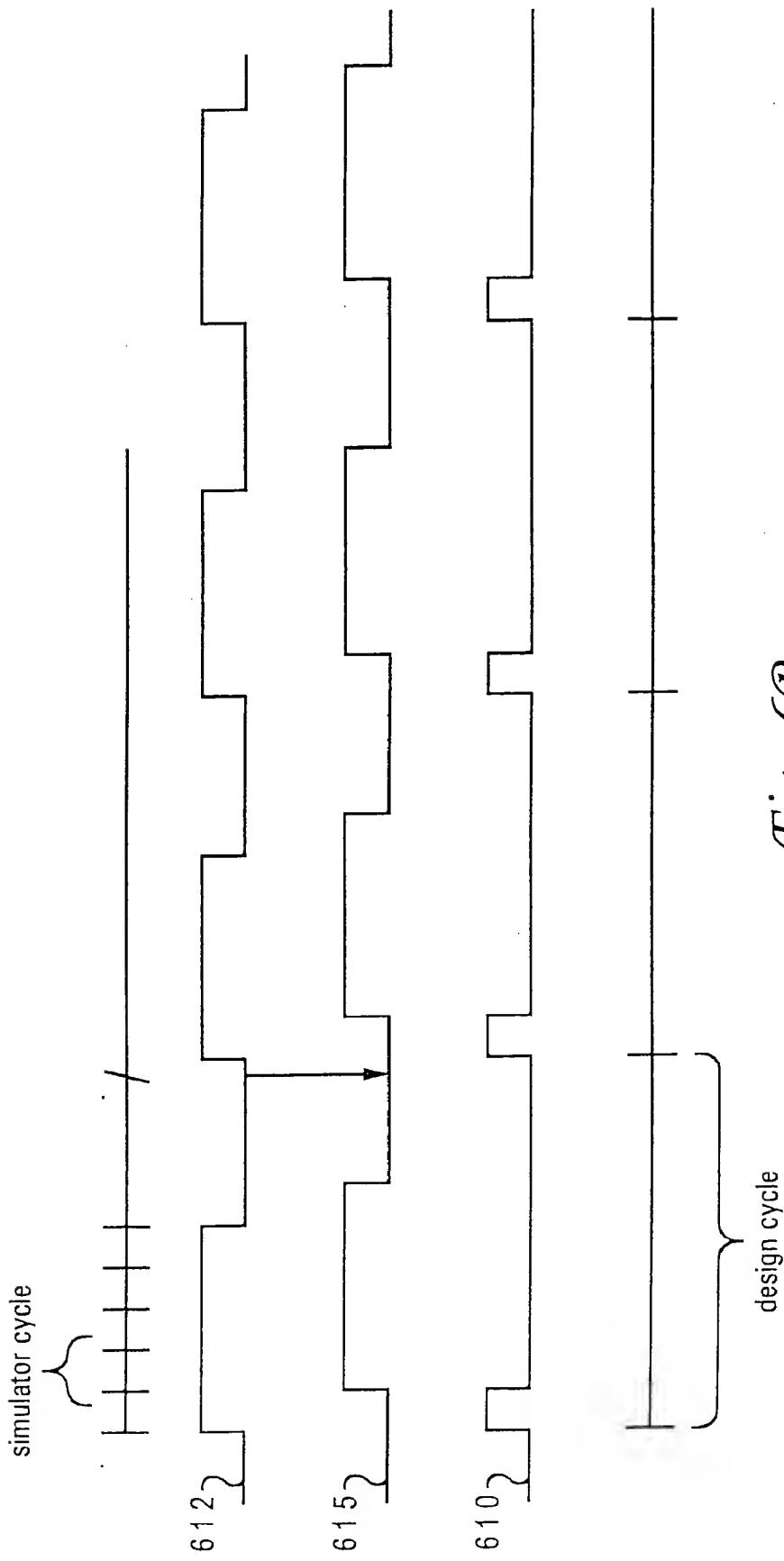


Fig. 6B
Prior Art

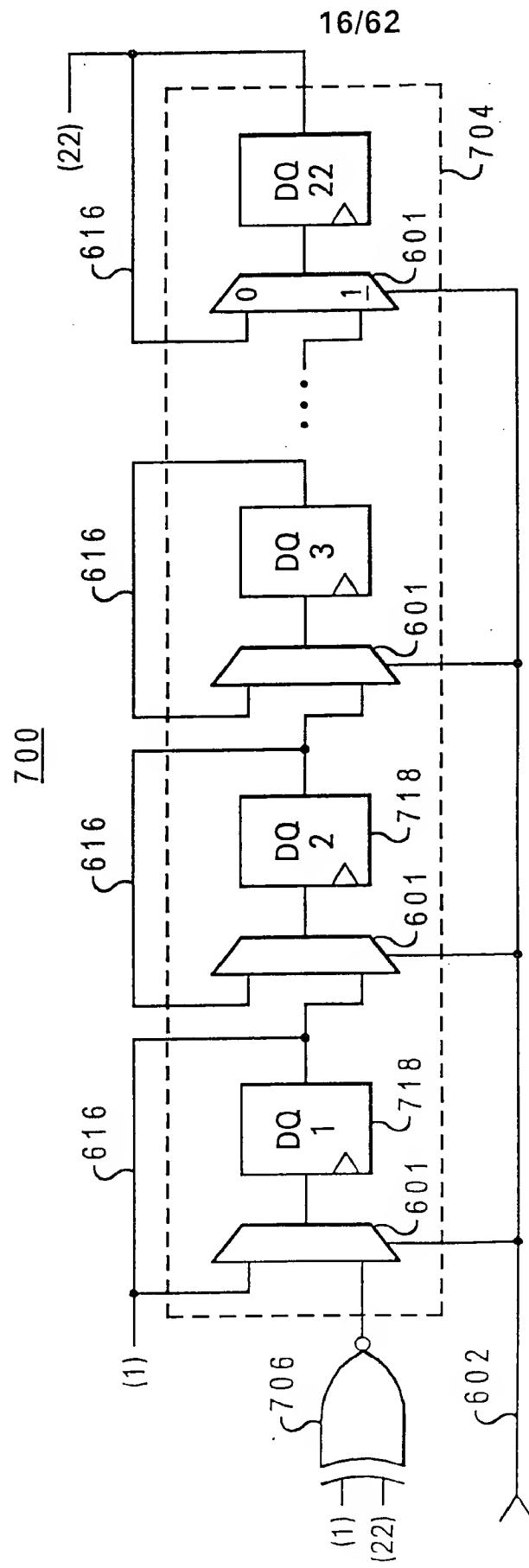


Fig. 7
Prior Art